What is claimed is:

1. An integrated circuit structure, comprising:

a capacitive electrode;

a dielectric underlying the capacitive electrode; and

an active region underlying the dielectric,

wherein the capacitive electrode and each conductive region between the capacitive electrode and the active region are formed of a conductive material having a hardness greater than a hardness of aluminum.

2. The integrated circuit structure of claim 1, wherein the capacitive electrode and each conductive region between the capacitive electrode and the active region are formed of a conductive material having a hardness at least as great as a hardness of the dielectric.

3. The integrated circuit structure of claim 1, further comprising:

a passivation layer over the capacitive electrode,

wherein the capacitive electrode and each conductive region between the capacitive electrode and the active region are formed of a conductive material having a hardness at least as great as a hardness of the passivation layer.

4. The integrated circuit structure of claim 1, wherein the capacitive electrode and each conductive region between the capacitive electrode and the active region are formed of tunsten.

5. The integrated circuit structure of claim 4, further comprising:

a tungsten via beneath the capacitive electrode.

6. The integrated circuit structure of claim 5, further comprising:

a tungsten interconnect beneath the via.

7. The integrated circuit structure of claim 6, further comprising:

a tungsten contact between the interconnect and the active region.

8. The integrated circuit structure of claim 7, wherein the active region is a gate electrode.

9. An integrated circuit structure, comprising:

an active region;

a dielectric overlying the active region and having a contact opening therethrough;

a tungsten contact within the contact opening;

a tungsten metal region overlying the contact and a portion of the dielectric;

an interlevel dielectric overlying the tungsten metal region and the dielectric and having an opening therethrough;

a tungsten via within the opening through the interlevel dielectric; and

a tungsten capacitive electrode overlying the tungsten via and a portion of the interlevel dielectric, wherein the capacitive electrode is electrically connected to the active region by the contact, the metal region, and the via.

10. The integrated circuit structure of claim 9, further comprising:

an oxide over the capacitive electrode and the interlevel dielectric adjacent the capacitive electrode;

a passivation layer including a silicon nitride layer and a silicon carbide layer over the oxide; and

tungsten ESD protection within the passivation layer.

11. An integrated circuit, comprising:

an array of capacitive electrodes in a central portion of the integrated circuit; and

ESD protection devices and contact pads around a periphery of the integrated circuit,

wherein the capacitive electrodes and every metallization region beneath the array of capacitive electrodes within the central portion of the integrated circuit is formed of a material having a hardness greater than aluminum while at least one metallization region beneath an ESP protection device or contact pad is formed of aluminum.

12. The integrated circuit of claim 11, wherein every metallization region within the central portion of the integrated circuit is formed of tungsten.

13. The integrated circuit of claim 12, further comprising:

tungsten ESD protection above and between capacitive electrodes within the array of capactive electrodes and within the central portion of the integrated circuit, wherein each capacitive electrode within the array is formed of tungsten;

tungsten vias beneath each capacitive electrode;

tungsten interconnects beneath each tungsten via;

tungsten contacts beneath each tungsten interconnect; and

active regions beneath each tungsten contact.

14. A method of forming a scratch resistant integrated circuit structure, comprising:

forming an active region;

forming a dielectric overlying the active region; and

forming a capacitive electrode overlying the dielectric, wherein the capacitive electrode and each conductive region between the capacitive electrode and the active region are formed of a conductive material having a hardness greater than a hardness of aluminum.

15. The method of claim 14, wherein the capacitive electrode and each conductive region between the capacitive electrode and the active region are formed of a conductive material having a hardness at least as great as a hardness of the dielectric.

16. The method of claim 14, further comprising:

forming a passivation layer over the capacitive electrode,

wherein the capacitive electrode and each conductive region between the capacitive electrode and the active region are formed of a conductive material having a hardness at least as great as a hardness of the passivation layer.

17. The method of claim 14, wherein the capacitive electrode and each conductive region between the capacitive electrode and the active region are formed of tunsten.

18. The method of claim 17, further comprising:

forming a tungsten via beneath the capacitive electrode.

19. The method of claim 18, further comprising:

forming a tungsten interconnect beneath the via.

20. The method of claim 19, further comprising:

forming a tungsten contact between the interconnect and the active region.

1 21. The method of claim 20, wherein the active region is a gate electrode.

22. A method of forming an integrated circuit structure, comprising:

forming an active region;

forming a dielectric overlying the active region and having a contact opening therethrough;

forming a tungsten contact within the contact opening;

forming a tungsten metal region overlying the contact and a portion of the dielectric;

forming an interlevel dielectric overlying the tungsten metal region and the dielectric and having an opening therethrough;

forming a tungsten via within the opening through the interlevel dielectric; and

forming a tungsten capacitive electrode overlying the tungsten via and a portion of the interlevel dielectric, wherein the capacitive electrode is electrically connected to the active region by the contact, the metal region, and the via.

23. The method of claim 22, further comprising:

forming an oxide over the capacitive electrode and the interlevel dielectric adjacent the capacitive electrode;

forming a passivation layer including a silicon nitride layer and a silicon carbide layer over the oxide; and

forming tungsten ESD protection within the passivation layer.

24. A method of forming a scratch resistant integrated circuit structure, comprising:

forming a plurality of active regions;

forming a dielectric over the plurality active regions; and

forming an array of capacitive electrodes overlying the dielectric of a conductive material having a hardness at least as great as a hardness of the dielectric.

25. The method of claim 24, wherein the step of forming an array of capacitive electrodes overlying the dielectric of a conductive material having a hardness at least as great as a hardness of the dielectric further comprises:

forming the array of capacitive electrodes of a conductive material having a hardness at least as great as a hardness of a passivation layer overlying the array of conductive electrodes.

26. The method of claim 24, wherein the step of forming an array of capacitive electrodes overlying the dielectric of a conductive material having a hardness at least as great as a hardness of the dielectric further comprises:

forming the array of capacitive electrodes of tungsten.

27. The method of claim 24, further comprising:

forming each metallization region between the array of capacitive electrodes and the plurality of active regions of a conductive material having a hardness at least as great as the hardness of the dielectric.